Verilog: Simulation and Synthesis
Implementing in FPGAs

First Day

Introduction to Verilog
- Necesidad e importancia de HDLs
- Concepts of top-down design
- Abstraction levels of Verilog
- Basic blocks of Verilog
- Hierarchical designs

Basic Concepts
- Modules, port, reg and net declarations
- Structural model
- Data flow model
- Behavioral model
- Intro to Simulation
- Intro to the ISE (Xilinx) environment

Verilog Syntax and Semantics
- Data types
- Attributes
- Numbers and logia values
- Arrays. Multidimensional arrays

Procedures, Statements and Operators
- Operators
- Operands
- Procedural blocks
- Full case and Parallel case
- Conditional operator '?'
- Combinational logia generations
- Intro to Test Bench
- Simulation using ISE
- Lab: Combinational logic coding

Second Day

RTL Models of Sequential Logic
- Blocking and non-blocking statements
- Sequential statements
- Generating sequential logic
- Modeling RAMs and ROMs
- Lab: Coding for Sequential and Combinatorial logic

Test Benches
- Importance of a good Test Bench
- Stimulus generations: signals & clocks
- Use of System Tasks and Functions
- Compilation Directives
- Test Bench examples
- Running simulation with ISE or ModelSim

Tasks and Functions
- Tasks
- Functions
- Use of multiples .v source files
- Lab: Use of Tasks and Functions

Synthesis of Finite State Machines (FSM)
- Verilog to model and synthesize Fumes
- Verilog code for the different FSM styles
- Vantages and disadvantages of the different FSMs
- State code assignment: manual/automatic
- Lab: Coding FSMs

Third Day

Digital Design Synthesis with Verilog
- Synthesis Syntax, Attributes and Directives
- Inferring specific components
- Lab: Use of XST (ISE) and/or Synplify Pro

Programmable Logic Devices
- Complex Programmable Logic Device (CPLD)
- Lattice Macho. Xilinx 9500.
- Field Programmable Gates Array (FPGA)
- Xilinx FPGAs. Spartan and Virtex 2
- Top-down design with ISE
- Understanding XSE reports
- Inferring specific Xilinx FPGA component
- Instantiating specific Xilinx FPGA component
- Intro to Performance improvement
- Gate level simulation
- Lab: Implementing a Complex Digital Design into a Xilinx FPGA